AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings of claims in the application.

LISTING OF CLAIMS:

Claim 1 (previously presented) A testing method for semiconductor integrated circuits wherein, in the testing method testing by a semiconductor testing apparatus having a comparison judgment circuit judging
a semiconductor integrated circuit integrated with a plurality of DA converters and a base voltage generation circuit determining the gradation output voltage characteristics,
by comparison of the gradation output voltages and reference voltages, wherein
the gradation level intervals to be the test objects are decided by the setting of different voltages to be applied at the base power supply input terminals of said base voltage generation circuit; and
said voltages are supplied at and between said base power supply input terminals from said semiconductor testing apparatus; and
by assigning correspondence between the input gradation data signals of the gradation levels of that interval, and the gradation output voltages,
the gradation output voltage testing through said semiconductor testing apparatus is made to be digital judgment.

Claim 2 (previously presented) A testing method for semiconductor integrated circuits according to claim 1, wherein,
according to the voltages provided at and between the base power supply input terminals from said semiconductor testing apparatus, said base voltage generation circuit increases or decreases the neighboring gradation output potential differences of every analog voltage output of said semiconductor integrated circuit.

Claim 3 (previously presented) A testing method for semiconductor integrated circuits according to claim 1, wherein,

by assigning correspondence between the voltage settings provided from said semiconductor testing apparatus and the input data, said DA converters and the base voltage generation circuit selectively test the output levels of the analog voltage outputs.

Claim 4 (previously presented) A testing method for semiconductor integrated circuits according to claim 1, wherein,
proving of the reliability of the test accuracy is made possible by treating the mutual relationship between the computation of the input data corresponding to every output voltage level and of the expectation values of the output voltages in the semiconductor integrated circuit specification and the setting of the output voltage expectation value levels, and
the voltage judgment value levels of said comparison judgment circuit carrying out the judgment of the output voltages, and
the change of the setting of the test numbers with time,
altogether as address or parameter management.

Claim 5 (previously presented) A testing device for semiconductor integrated circuits, wherein, in a judging testing apparatus, through a comparison judgment circuit, a semiconductor integrated circuit integrated with a plurality of DA converters and a base voltage generation circuit determining the gradation output voltage characteristics, by comparison of said gradation output voltages and reference voltages, wherein different voltages are output to the base power supply input terminal for the end of one side of the gradation level interval being the test object of said semiconductor integrated circuit, and
the base power supply input terminal of the other end of said interval.

Claim 6 (previously presented) A testing device for semiconductor integrated circuits according to claim 5, wherein,
said voltages are output to more than two base power supply input terminals including the base power supply input terminal at the end of at least one side of the gradation level interval being the test object of the semiconductor integrated circuits.

Claim 7 (previously presented) A testing device for semiconductor integrated circuits according to claim 5, wherein,

base power supply input terminals not connected with the semiconductor testing apparatus are disposed in the gradation level interval being the test object of the semiconductor integrated circuit.

Claim 8 (previously presented) A testing device for semiconductor integrated circuits according to claim 5, wherein,

more than two gradation level intervals being the test objects of the semiconductor integrated circuits are disposed.

Claim 9 (New) A testing device for semiconductor integrated circuits, comprising:

a semiconductor integrated circuit integrated with a plurality of base power supply input terminals, a base voltage generation circuit having a Gamma correction resistance, and a plurality of D/A converters, generating gradation output voltage characteristics; and

a comparison judgment circuit for comparing gradation output voltages and reference voltages, for a plurality of gradation output voltages in parallel simultaneously.

Claim 10 (New) A testing method for semiconductor integrated circuits comprising:

setting of an upper limit level and lower limit level of graduation output voltage level intervals in between base power supply terminals being test objects;

second step of setting a test generation number and a gradation output voltage expectation value level for a graduation output voltage level;

sequentially testing all graduation output voltage levels in between base power supply terminals for each graduation level;

judging whether a test result at a graduation output voltage level is a failure, and if so ending the test; and

repeating the second step of setting, sequentially testing and judging until a designated gradation level or test failure.